PATENT APPLICATION

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of

Terunao HANAOKA Group Art Unit: 2811

Application No.: 10/679,467

Filed: October 7, 2003 Docket No.: 117462

For: SEMICONDUCTOR WAFER, SEMICONDUCTOR DEVICE AND METHOD OF

MANUFACTURING THE SAME, CIRCUIT BOARD, AND ELECTRONIC EQUIPMENT

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450

Sir:

Pursuant to 37 CFR §1.56, the attention of the Patent and Trademark Office is hereby directed to the references listed on the attached PTO-1449. Unless otherwise indicated herein, one copy of each reference is attached. It is respectfully requested that the information be expressly considered during the prosecution of this application, and that the references be made of record therein and appear among the "References Cited" on any patent to issue therefrom.

- 1. This Information Disclosure Statement is being filed (a) within three months of the U.S. filing date of this non-CPA application, OR (b) before the mailing date of a first Office Action on the merits in the present application. No certification or fee is required.
- 2. English language Abstracts of the non-English language references are attached hereto.
- 3. A computer-generated English language translation of the following Japanese references has been obtained from the website of the Japanese Patent Office ([http://www.jpo.go.jp]), and is attached, but has not been reviewed for accuracy. See Reference 1 & 2.

Respectfully submitted

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Date: March 28, 2005

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INFORMATION DISCLOSURE STATEMENT												
(Use several sheets if necessary)				APPLICANT Terunao HANAOKA								
					FILING DATE October 10, 2003				GROUP 2811			
U.S. PATENT DOCUMENTS												
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	1	JP A 2000-311921 w/ abst. & trans.		7-2000	JAPAN							
	2	JP A 2000-340588 w/ abst. & trans	12-8	3-2000	JAPAN			·				
OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)												
					 							
												
												
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Date: March 28, 2005